REMARKS

Claims 11 and 12 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. It is believed the Examiner is relying on the "enablement" portion of 35 U.S.C. § 112 first paragraph rather than the "written description" portion. Applicants clearly had possession of the subject matter of claims 11 and 12 upon filing this application. A rejection based on "written description" is not proper when addressing claims as originally filed.

The Office Action also references enablement. With respect to enablement, the terms "broadside" and "compartmentally" are used to describe two different types of cache access. As described in paragraph [0019] a broadside access obtains the full content of the cache across compartments 112. As 8 compartments are used, each including 128 bits, the broadside read provides a 1024 bit trace signal. This terminology is known in the art as represented, for example, in U.S. Patent 4,317,168 and European Patent 763,795. A compartment access is access to one of the 8 compartments in the cache, resulting in reading or writing a 128 bit word as described in at least paragraphs [0018] and [0019]. Accordingly, Applicants submit that the specification does enable one of ordinary skill in the art to make and use the invention described in claims 11 and 12.

OK, in light of this explanation.

Claims 1, 3, 8, 10 and 13-17 were rejected under 35 U.S.C. § 102(b) as being anticipated by Assouad.

Claim 1 recites "in a system mode, using all of said cache memory as a data cache; in a trace mode; dividing said cache memory into a reduced-size cache memory and a trace array." Assouad fails to teach or suggest this feature. In applying Assouad, the Examiner considered the buffer memory 104 to correspond to the claimed cache. The buffer memory 104, however, is divided into data areas and a trace area as shown in Figure 6 and described in column 9, lines 15-39. There is no system mode in Assouad in which the entire buffer 104 is used for data cache. A portion of buffer memory 104 is dedicated to trace signals at all times, and thus Assouad fails to teach the two modes of operation as recited in claim 1.

For the above reasons, claim 1 is patentable over Assouad. Claims 3, 8, 10 and 13-15 depend from claim 1 and are patentable over Assouad for at least the reasons advanced with respect to claim 1. Claims 15 and 16 include features similar to those in claim 1 discussed above and are patentable over Assouad for at least the reasons advanced with respect to claim 1.

Claims 2 and 4-6 were rejected under 35 U.S.C. § 103 as being unpatentable over Assouad in view of Kirk. Kirk was relied upon for disclosing partitioning cache into equal halves, but fails to cure the deficiencies of Assouad discussed above with reference to claim 1. Thus, claims 2 and 4-6 are patentable over Assouad in view of Kirk for at least the reasons advanced with respect to claim 1.

Claim 9 was rejected under 35 U.S.C. § 103 as being unpatentable over Assouad in view of Fischer. Fischer was relied upon for disclosing a system on a chip environment, but fails to cure the deficiencies of Assouad discussed above with reference to claim 1. Thus, claim 9 is patentable over Assouad in view of Fischer for at least the reasons advanced with respect to claim 1.

Claim 7 was objected to and has been placed in independent form. Claim 18 was allowed. Applicants note that, pursuant to 35 U.S.C. § 112, sixth paragraph, claim 18 is directed to structure disclosed in the specification and equivalents thereof.

In view of the foregoing remarks and amendments, Applicants submit that the above-identified application is now in condition for allowance. Early notification to this effect is respectfully requested.

If there are any charges with respect to this response or otherwise, please charge

them to Deposit Account 09-0463 maintained by Applicants' Assignee.

Respectfully submitted,

By: _____

David A. Fox
Registration No. 38,807
CANTOR COLBURN LLP
55 Griffin Road South
Bloomfield, CT 06002
Telephone (860) 286-2929
Facsimile (860) 286-0115
Customer No. 23413

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